# Future Directions for Microsystems Technology


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**Microsystems Technology Office**

**Microsystems Technology Symposium**
**March 7, 2007**

# Report Documentation Page

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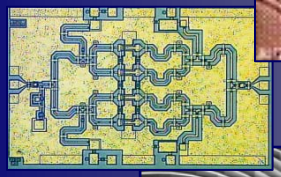
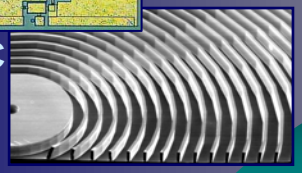
# Microsystems Technology Office: Enabling Future Capability

## Sense

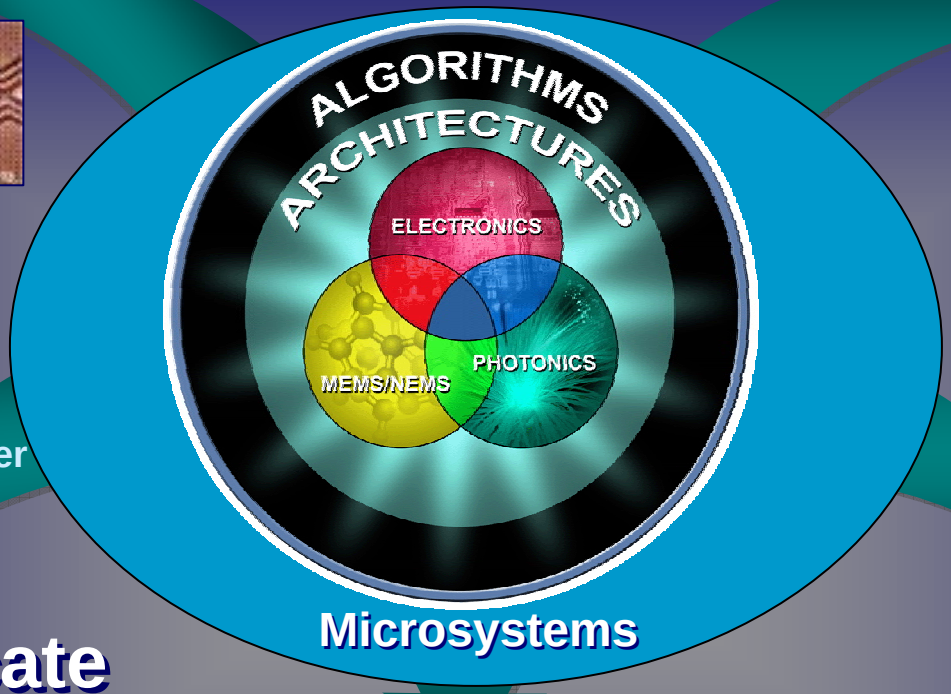
Microbolometer



RF MMIC

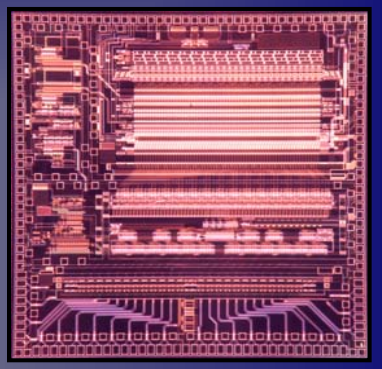


Micro Gas Analyzer



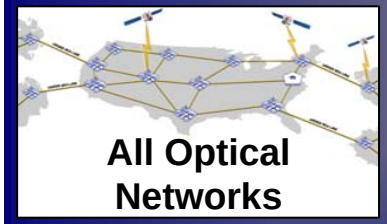

Microsystems

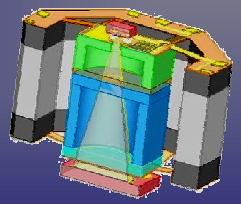
## Process



Digital Integrated Circuits

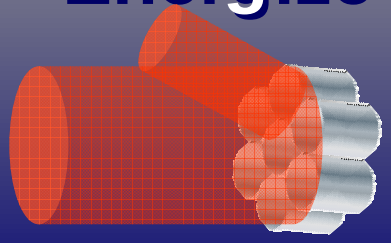
## Communicate



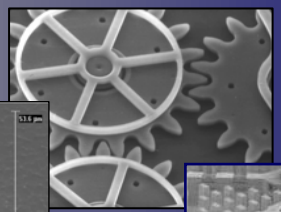
Chip Scale Atomic Clock

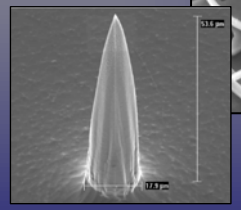
## Energize

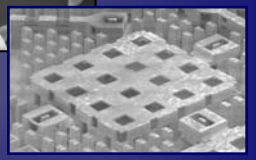


Adaptive Photonic Phase-Locked Elements

## Actuate







MicroElectroMechanical devices

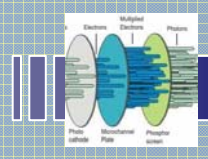
# Microsystems Technologies Impact on Warfighter

PAST

PRESENT

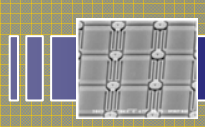
FUTURE

Night Vision



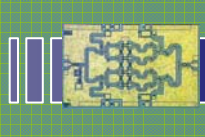
Improved Image Intensifier Tubes

Thermal Imaging



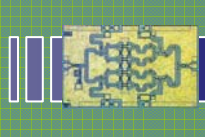
Uncooled LWIR FPAs

Communications

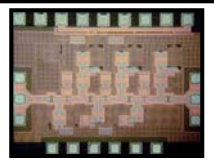


RF MMICs

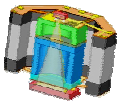
Geo-location



PCAR & AFPA

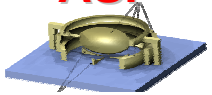


TEAM



CSAC

ASP



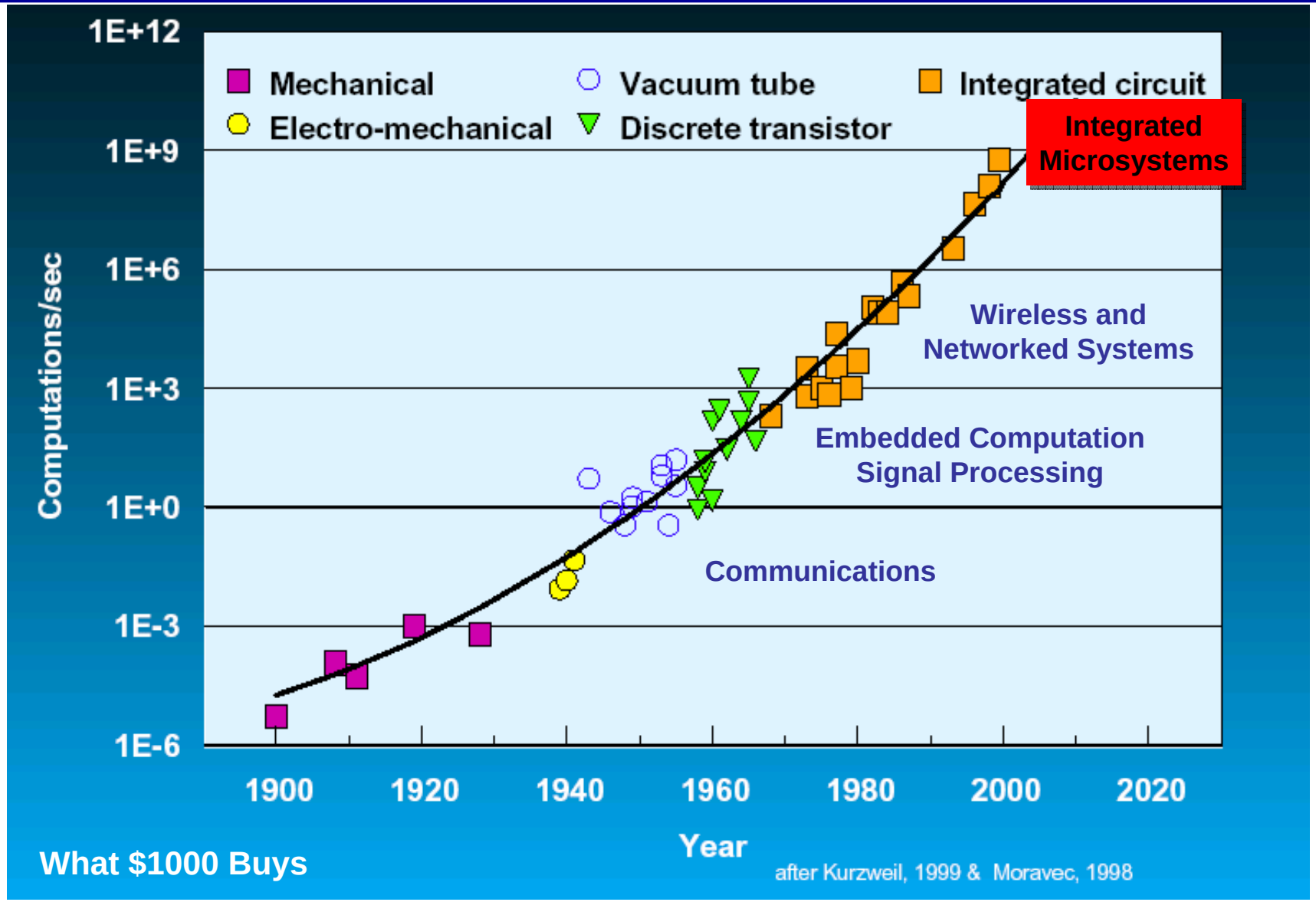
NGIMG

**The individual soldier's load is cumbersome, but advances in microsystems have enabled enhanced capabilities in a reduced overall form factor**

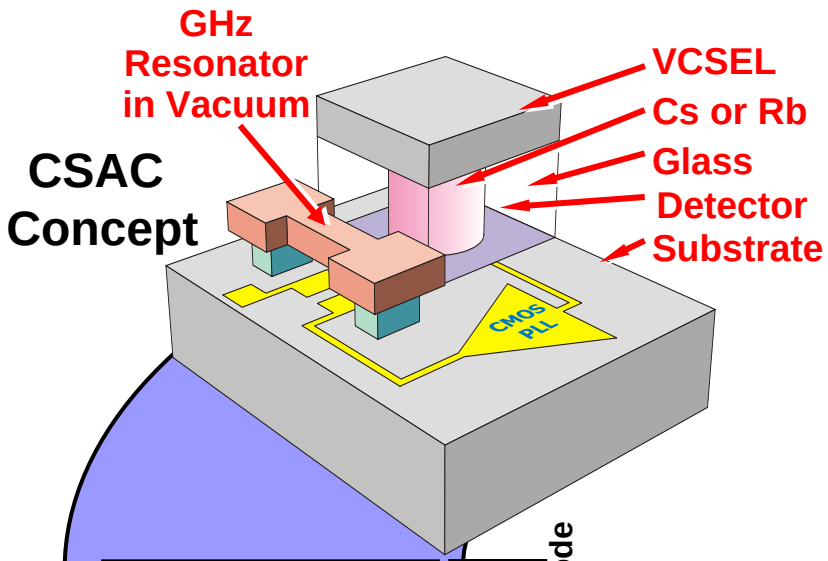
*Improved Performance*

*Reduced Package Size*

# Progression of Microtechnology



# Moving NanoScience to NanoTechnology: Chip Scale Atomic Clock

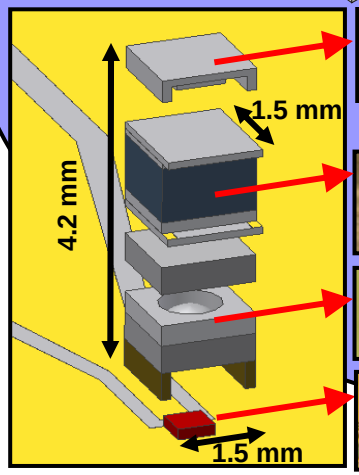


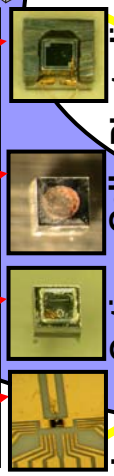

CSAC Concept

Example of Use: Radio System (SINCGARS)

Clock accuracy of 1s/10,000 yrs ⇒
16-hour re-synch interval or radio silence

Goal: Vol: 1 cm³
Power: 30 mW
Stab: 1s in 10k yrs

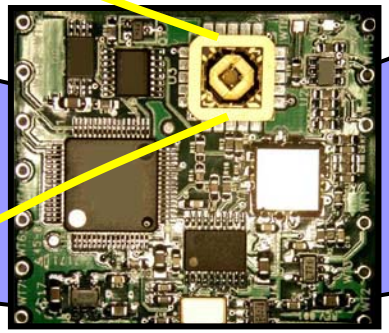


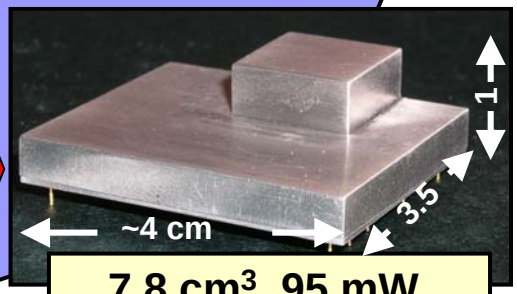

Physics Package

3.94 cm

3.5 cm



CSAC Breadboard




7.8 cm³, 95 mW,
5x10⁻¹¹ at 100 sec

Phase II CSAC Prototype

**Precision Time for Every Radio and Network Node**

# Future Microsystems Icons

- Chip Scale Atomic Clock
- 3D Electronics and Imagers
- All Optical Data Router
- 3rd Generation MMICs (WBG-RF)
- Analog-to-Information (Compressive Sensing)
- Micro Gas Sensors
- High Power Optical Phased Arrays
- High Power Electronics
- Personnel Navigation and Guidance
- Adaptive Microsystems
- Tactical Laser Weapons and Comms
- 0.25 V Logic

# Microsystems Technology Office: Enabling Future Capability

## Sense

Challenges:
Sensitivity
Linearity
Efficiency
Dynamic Range
Spectral Range

Micro Gas Analyzer

## Process

Challenges:
Power Dissipation
Complexity
Design
Latency

Digital Integrated Circuits

ALGORITHMS
ARCHITECTURE

Common Challenges:
Integration
Scaling
Power
Efficiency

Microsystems

## Communicate

Challenges:
Precision
Efficiency
Tuning
Dynamic Range

Clock

## Energize

Challenges:
Efficiency
Energy Density
Beam Quality

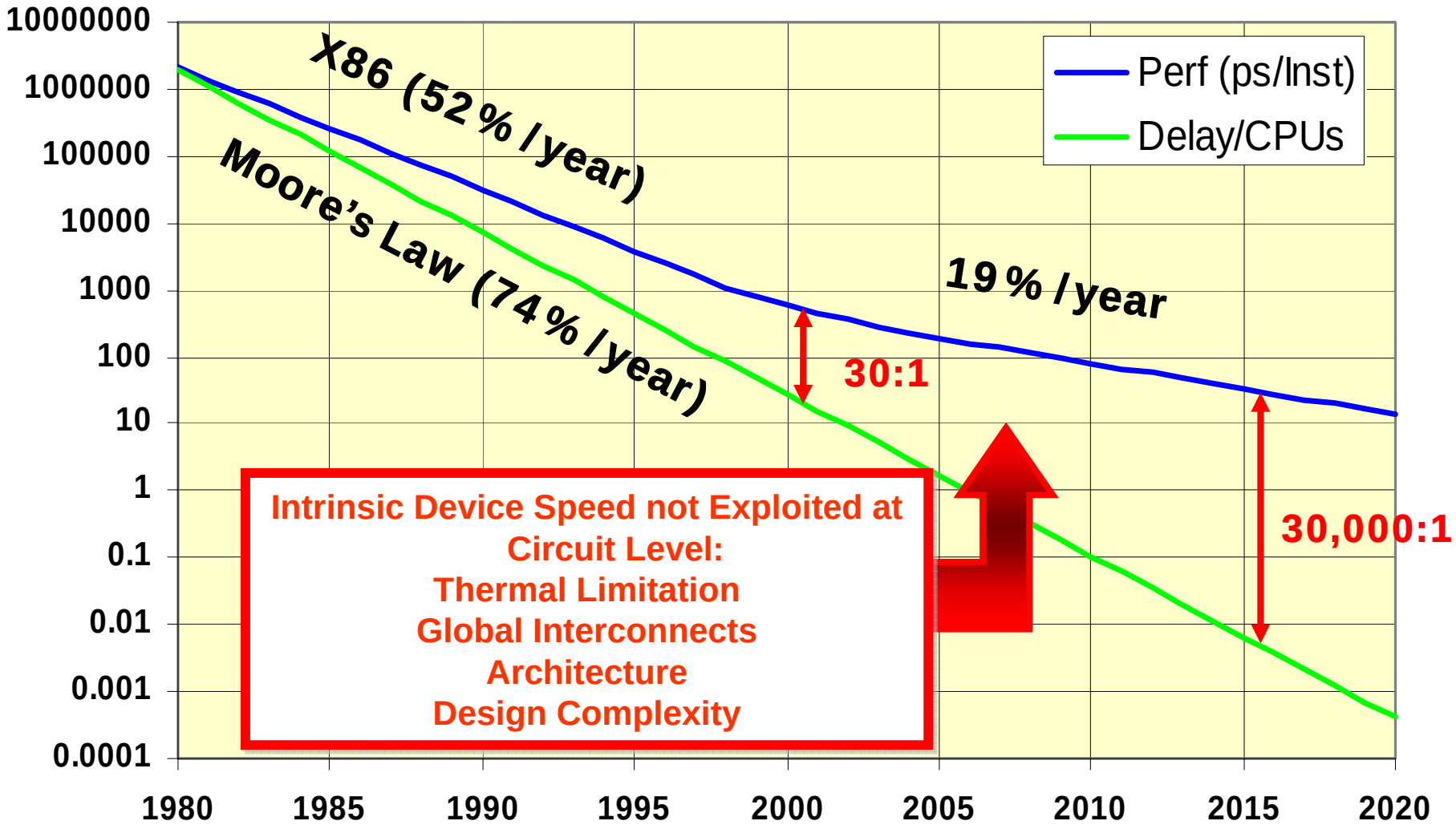
Adaptive Photonic Phase-Locked Elements

## Actuate

Challenges:
Accuracy
Precision
Robustness

MicroElectroMechanical devices

# Intrinsic Transistor Performance versus Circuit Speed

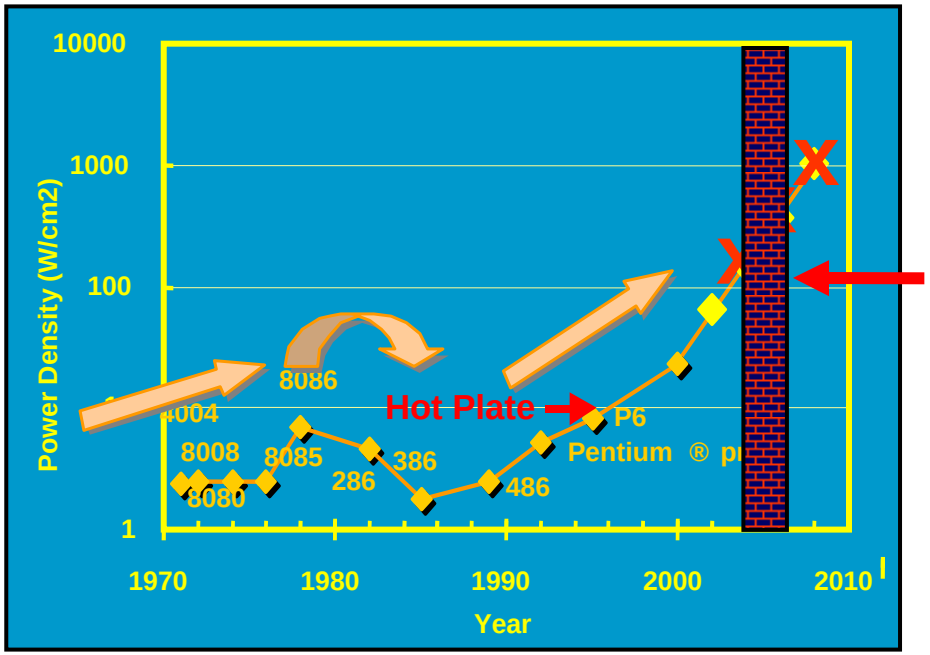



Source: ISAT Summer 2001 Study- *Last Classical Computer*;
Prof. Bill Dally (Stanford U) Study Lead

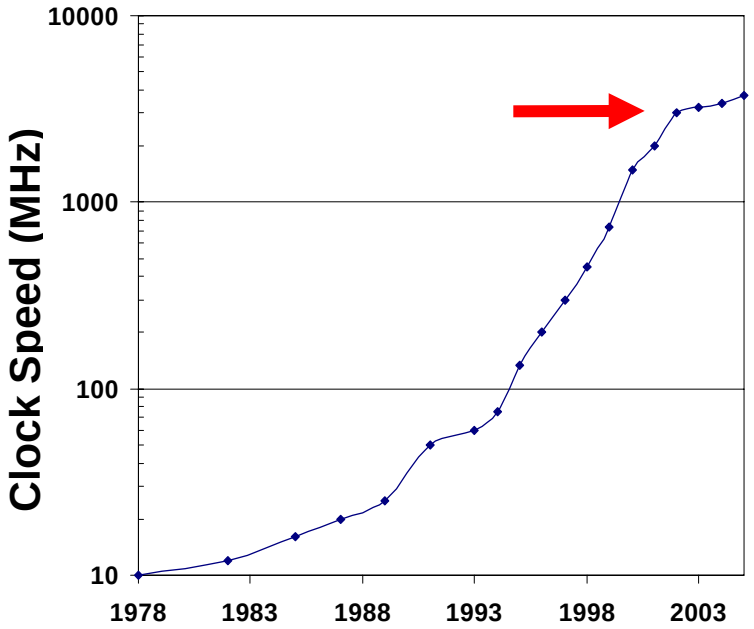
# Integrated Circuit Power

**Problem Statement: Conventional Si CMOS scaling is hitting a roadblock in heat dissipation.**

CMOS Microprocessor
Power Density Progression




Microprocessor Speed



# Integrated Circuit Power

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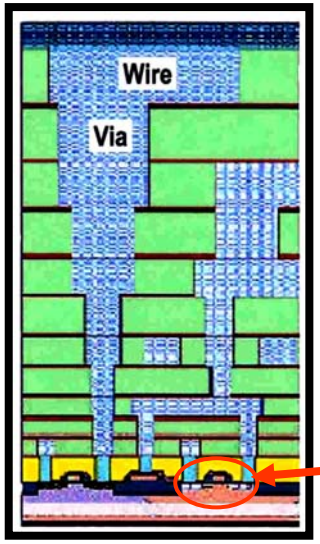
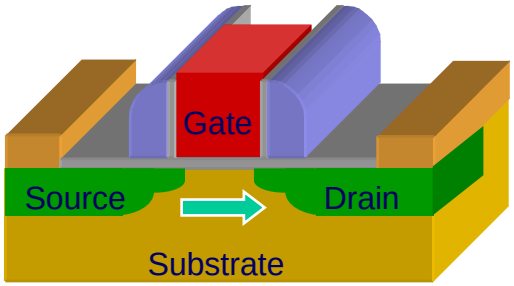
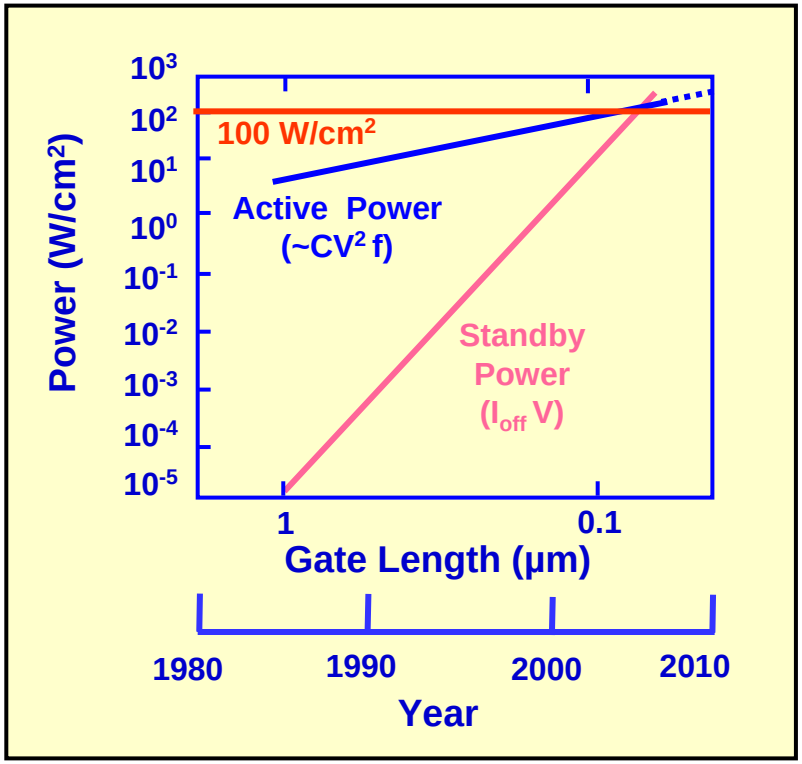



**Circuit Cross-Section**




**Silicon Transistor**

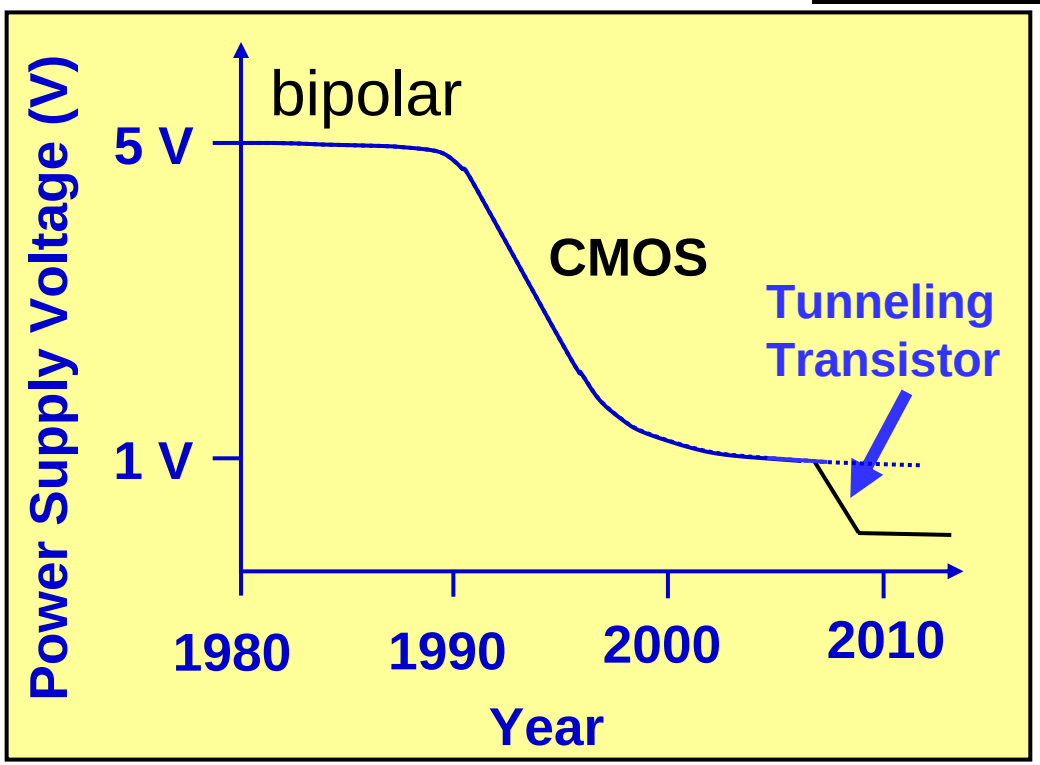
Components of Microprocessor Power

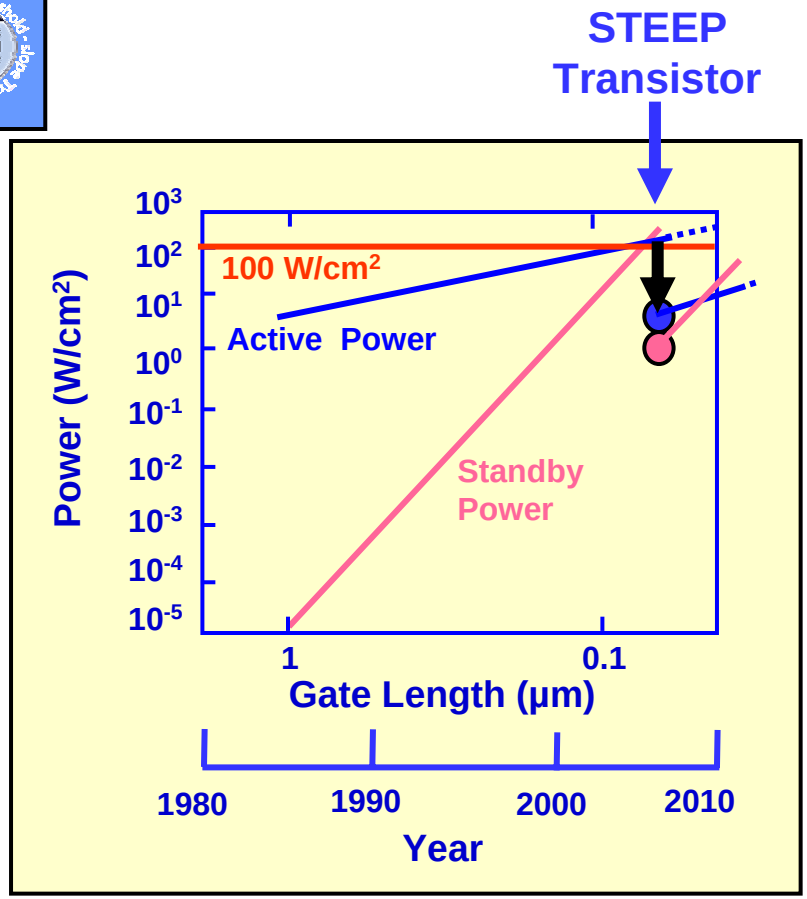



Transistor Power Loss:
- Active: Switching Loss ($0.5CV^2f$)
- Standby: Leakage Currents (IV)

Interconnect Power Loss:
- Wires Resistance (I2R)

# Trend in CMOS Active Power Voltage Scaling



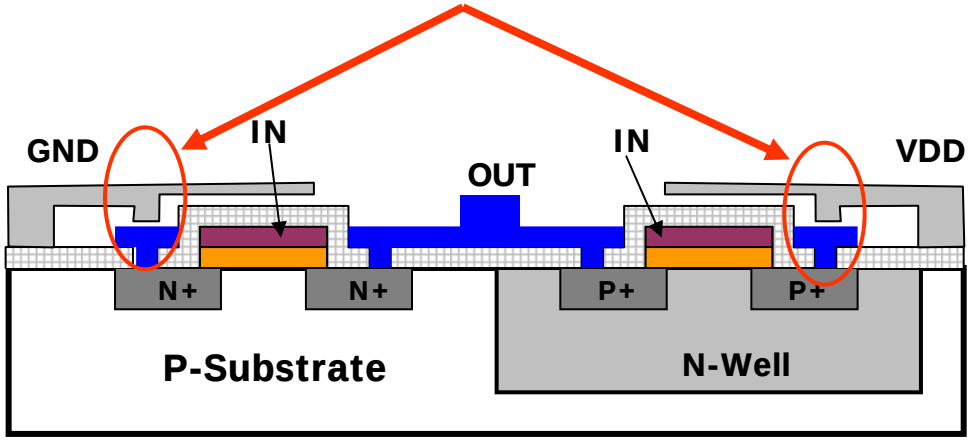




**Develop Steep Sub-threshold Slope Switch.**
**Reduce Operating Voltage from 1V to 0.25V: Reduce Active Power by 25x;**
**Reduce Standby Power by up to 100x**

# NanoElectroMechanical Switch: NEMS-tronics

**Objectives: Eliminate standby power in electronics to enable longer battery life and higher performance circuits.**

**Introduce switchable, insulating, "air gap" between power and ground**

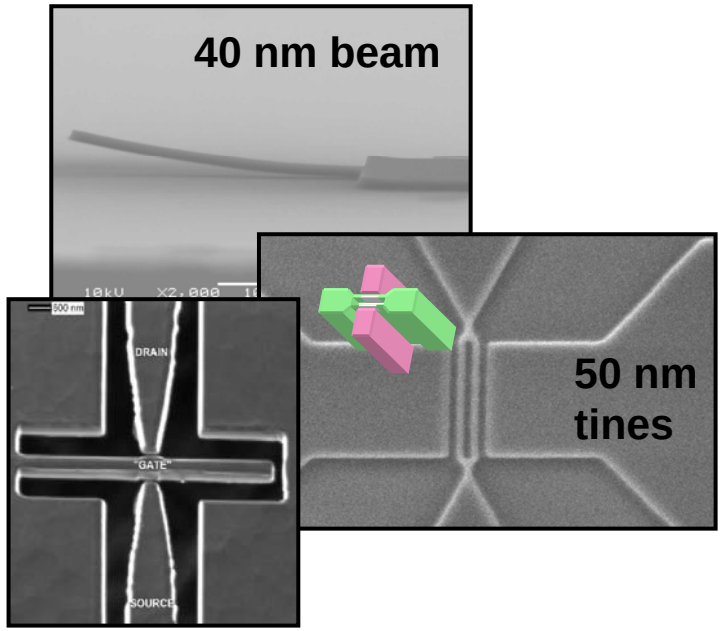



**Hybrid NEMS/CMOS Device integration**

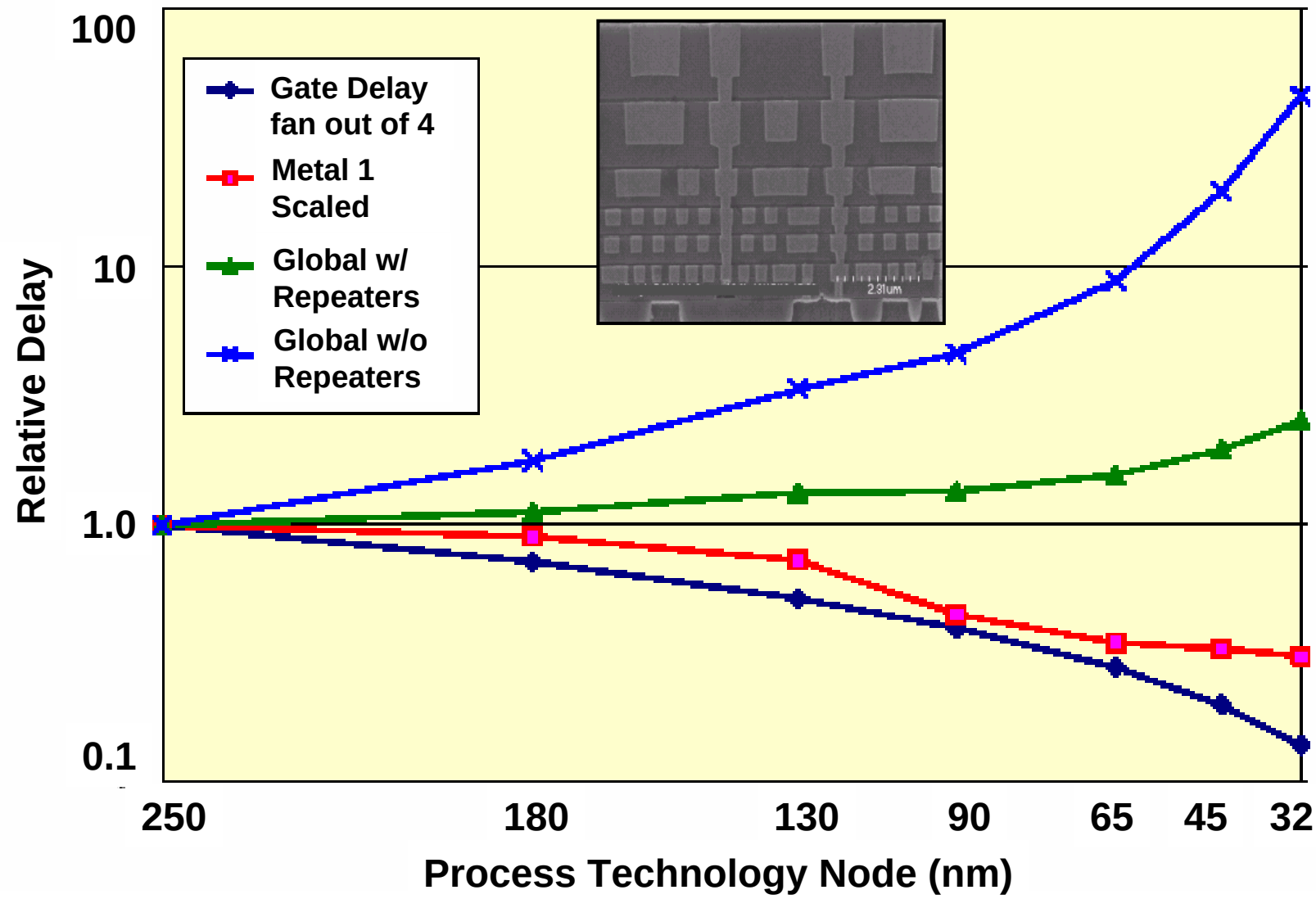
Key Technical Challenges for Mechanical Switch:

- fast (GHz switching)
- small (<100 nm on a side)
- robust (billions of cycles)

**Switch Concepts**

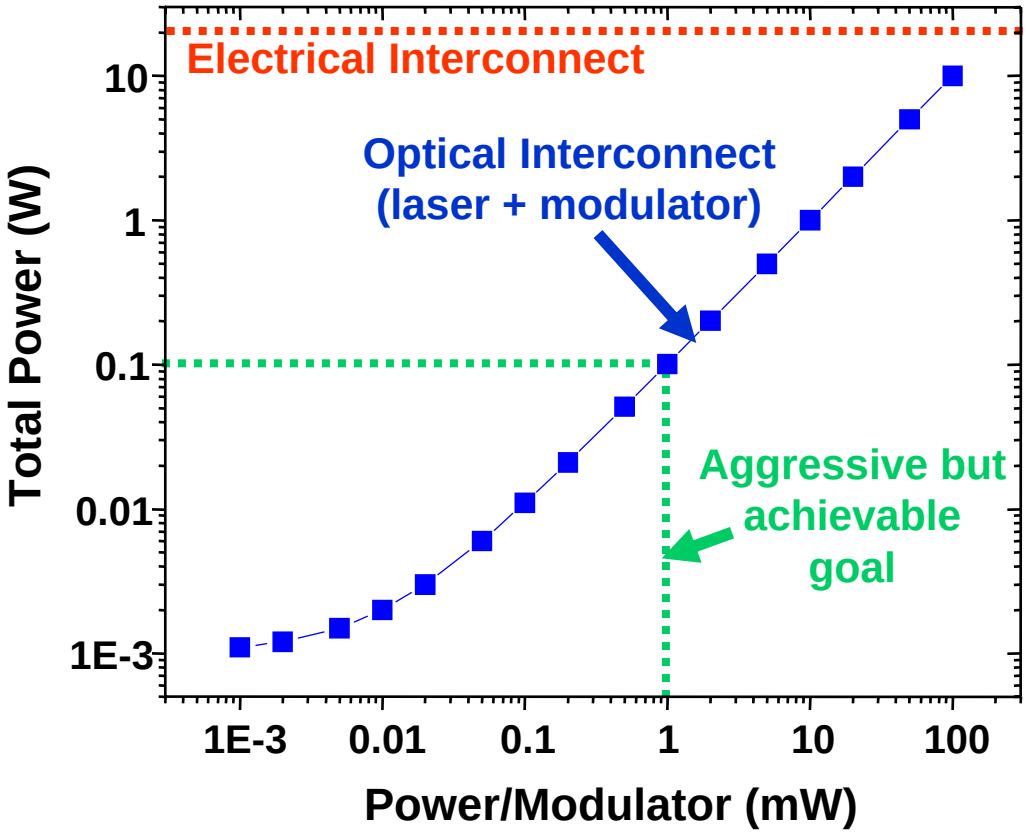


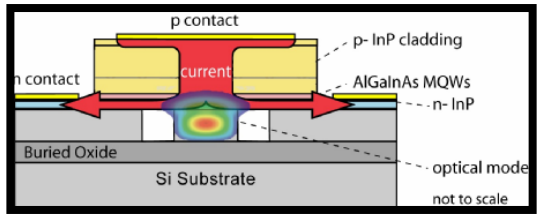
# Global Interconnects Limit Performance

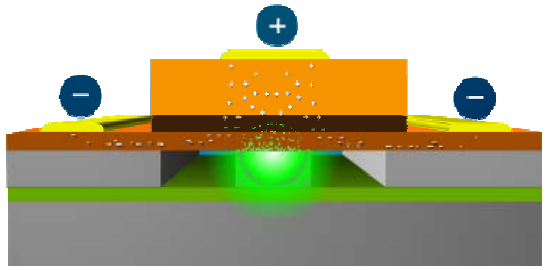


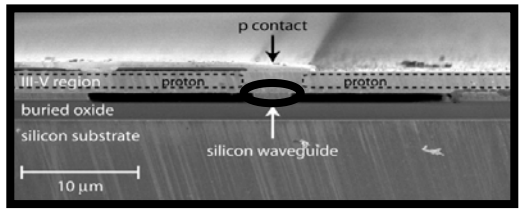
# On-Chip Optical Networks?

## 4 Tb/s Global Interconnect Capacity



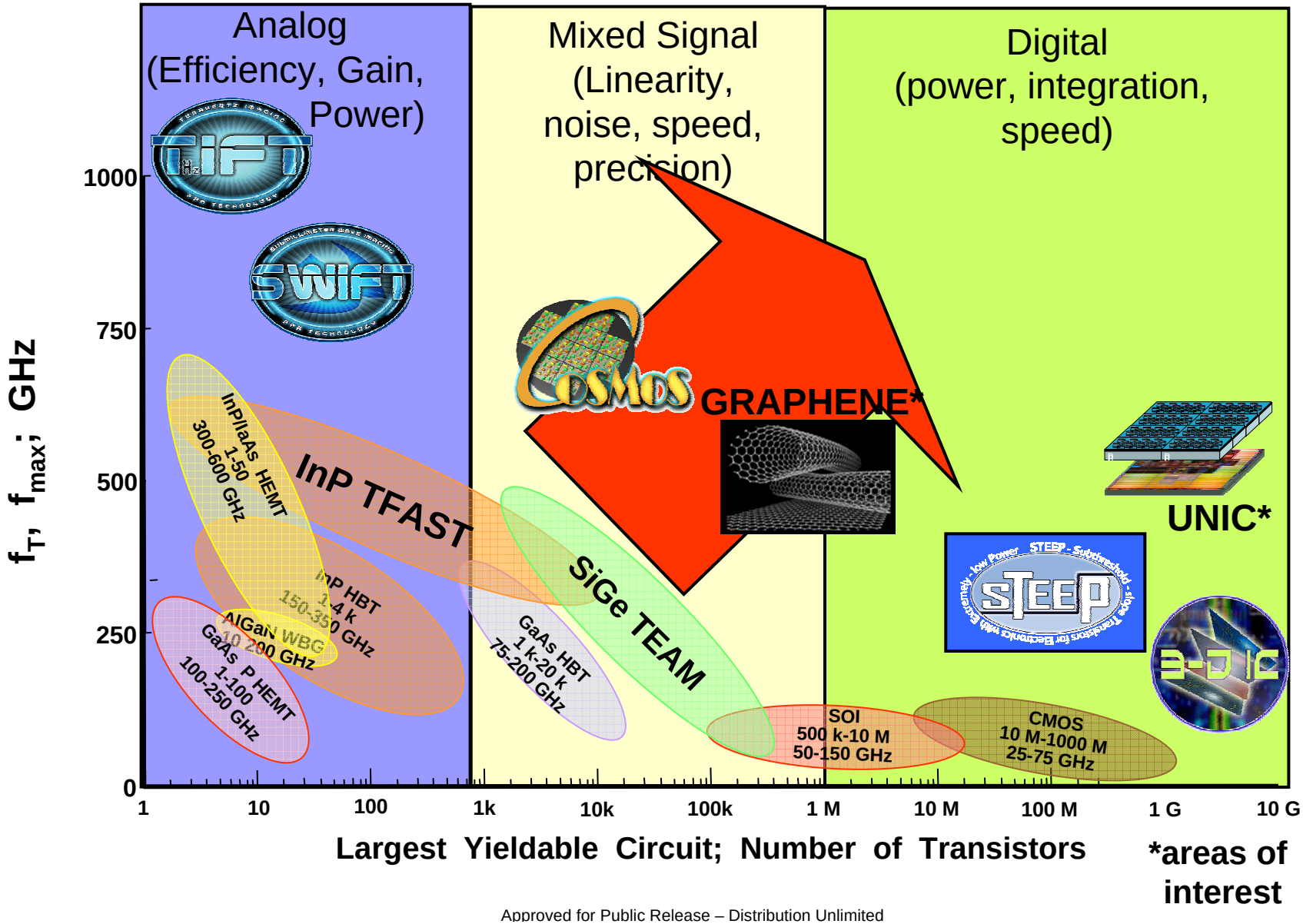




**Hybrid Laser on Silicon: Photons Directly Coupled into Si Waveguide**

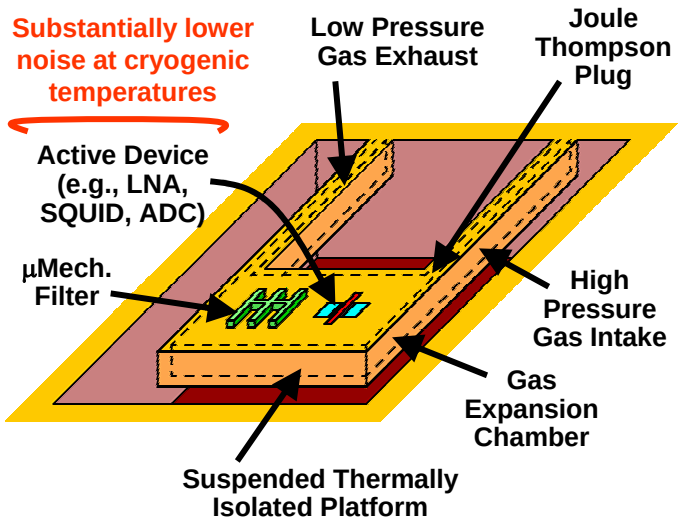
**The high speed and low power of optical global interconnects will reduce power dissipation and enable higher performance circuits.**

# Beyond Digital Electronics

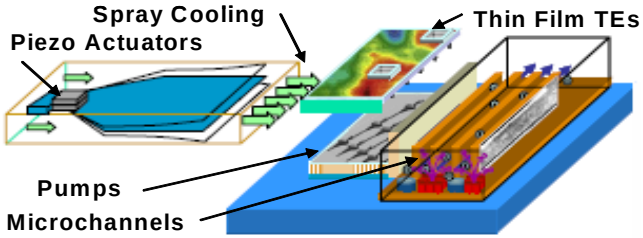


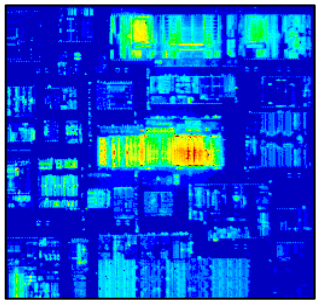
# Removing Thermal Limitations

## Micro-Cryo Coolers




## Site Specific Thermal Management*

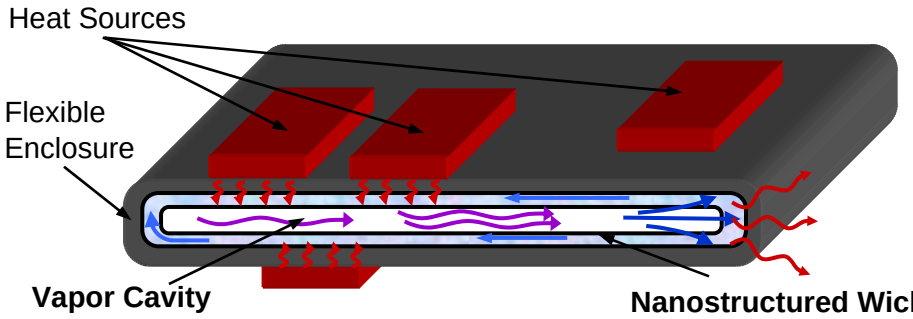


IC temperature profile

## Thermal Ground Plan*

### NanoFluidic Thermal Substrates




***Not Current DARPA Programs**

# Exploiting Photonics Technology


Bandwidth

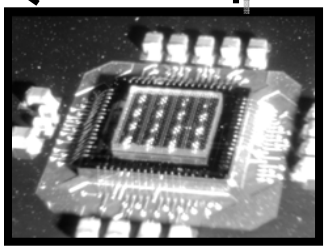
Zero Crosstalk

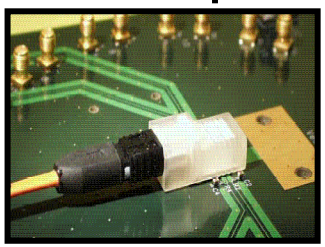
Sensing

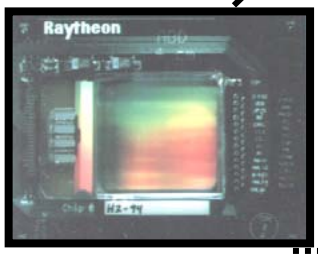
**Application Pull**

**MTO**

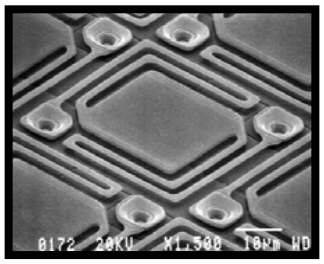
**Technology Push**

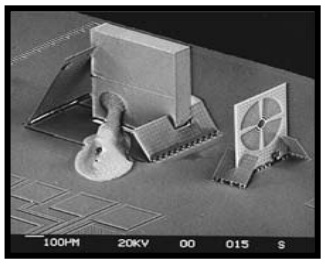


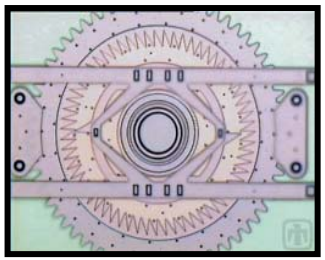





Module

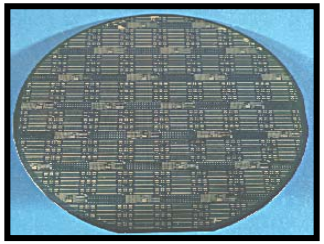


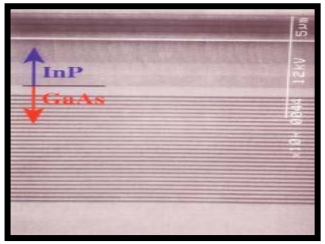



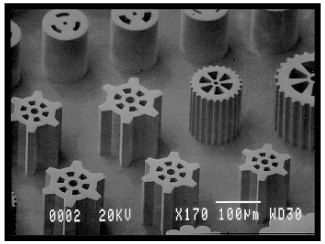



Device

Fabrication






Materials

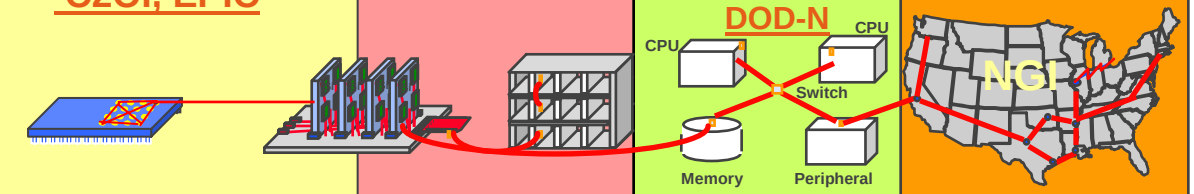
# Photonic Data Links

University Programs:

University Opto Centers

Ultra Photonics: MOST

| Network Scale: | Chip | Board | Platform | Global |
|---|---|---|---|---|
| MTO Program: (active/complete) | CS-WDM, C2OI, EPIC | VLSI-P | OMNET, OCDMA, DOD-N | BIT |
| Photonic Technologies: | • Heterogeneous O/E Integration<br>  • Dense 2-D<br>  • Waveguide & Free Space<br>  • WDM | • GaAs based O/E<br>• Si electronics<br>• Freespace<br>• 2-D arrays<br>• DOE/VCSELs | • GaAs based O/E<br>• VCSELs<br>• mm Fiber/POF<br>• Gb/s<br>• Serial/parallel | • InP based O/E<br>• SM-glass Fiber<br>• Very high speed TDM<br>• WDM |




Accessing Quantum Systems

1Å 10 Å 100 Å 1000 Å

1nm 1μm 1mm 1m 1km 1000km

VLSI Today (2005): 1B transistors/cm$^2$

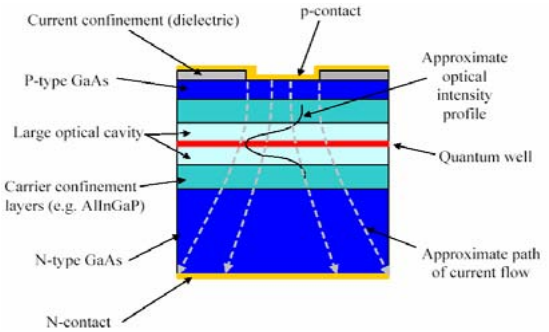
Projected Limits to CMOS (2015: 10B transistor/cm$^2$)

Atomic Scale

# Semiconductor Lasers

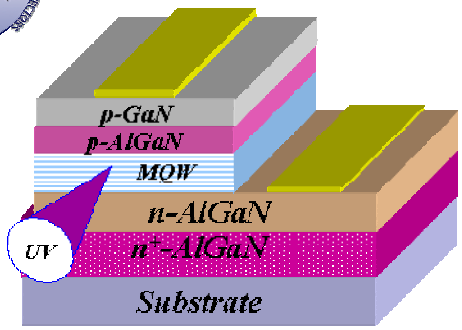
## Efficiency






## Ultra Violet

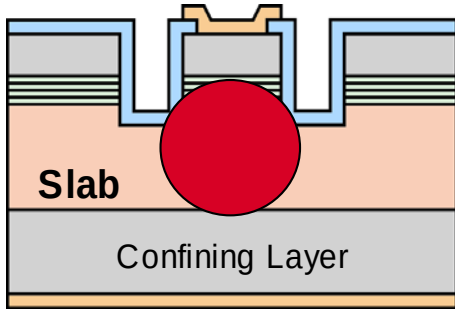
SAIL




## Robust/High Brightness

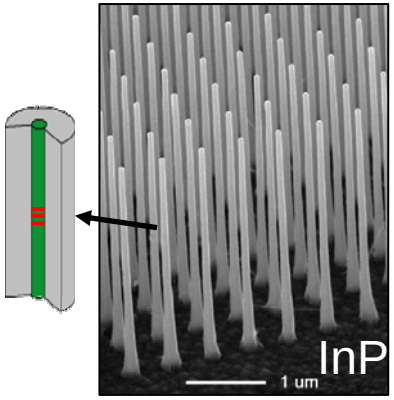
COCHISE

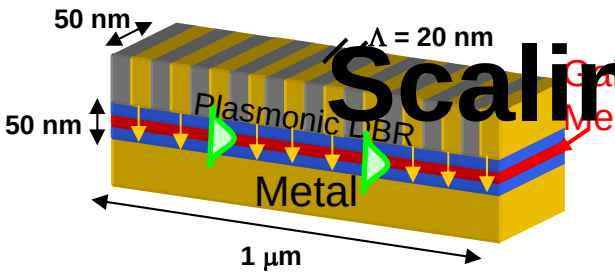
**Single Slab-Coupled Optical Waveguide Laser (SCOWL)**




## Nano-Scale Lasers

NACHOS




# Efficiency
# Wavelength
# Beam Quality
# Stability/Noise
# Lifetime
# Scaling

# Future Laser Directions

- **Efficient Green Lasers**
- **High lifetime and high efficiency**
- **Narrow linewidth, high power fiber lasers**

# Focal Plane Arrays


SHORT-WAVE


MEDIUM-WAVE


LONG-WAVE

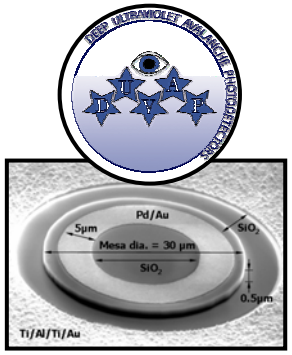

THz

Operating Wavelength

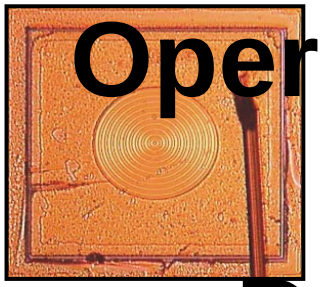
Sensitivity

Dynamic Range

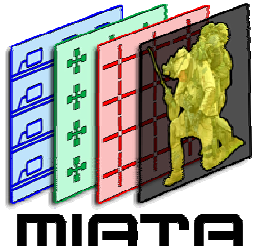
Operating Temperature

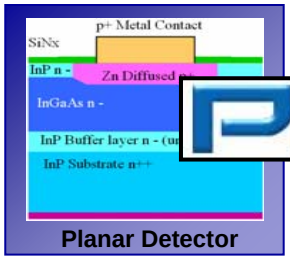


DUVAP
(0.5 μm)

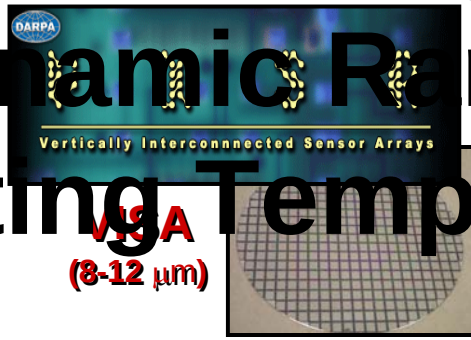

HOT-MWIR
(3-5 μm)

(8-12 μm)



MIATA

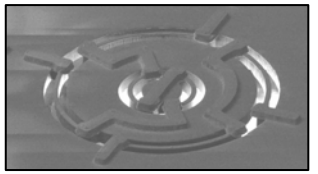


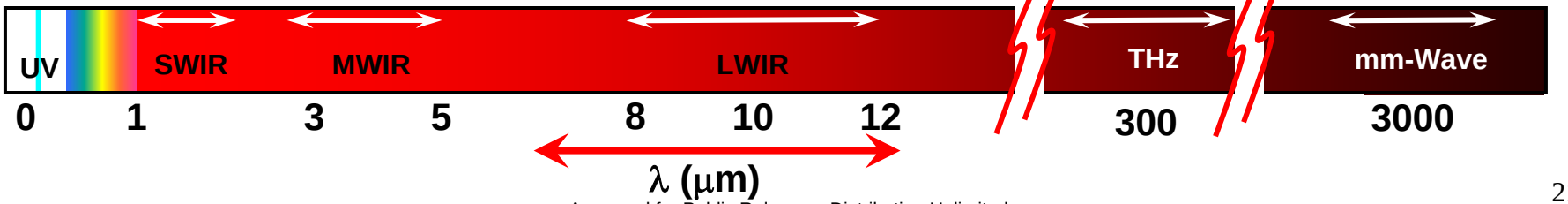

(1-2 μm)



VISA
(8-12 μm)


TIFT
(THz)

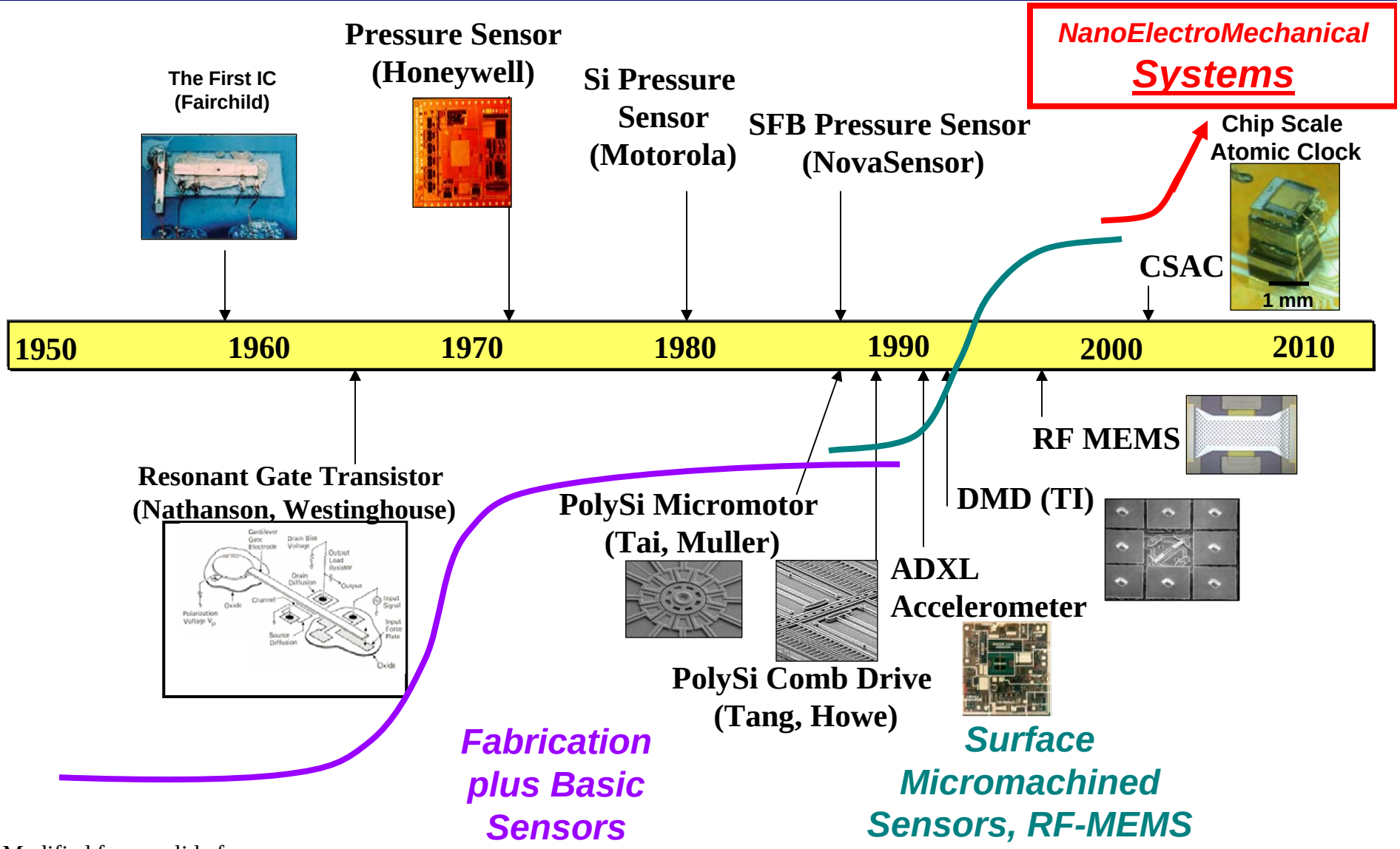

MIATA
(mm-Wave)



# Future FPA Directions

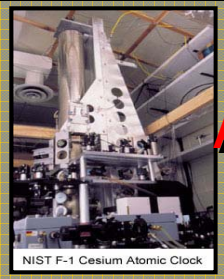
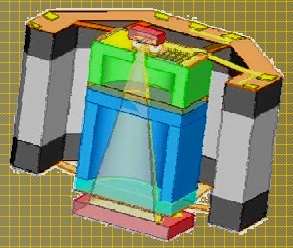
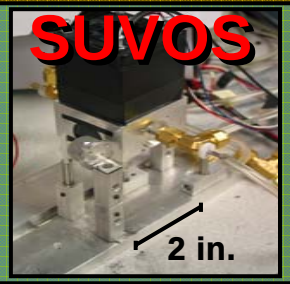
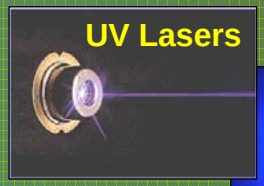
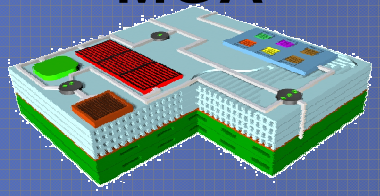
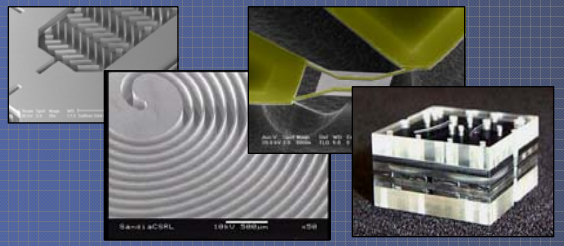
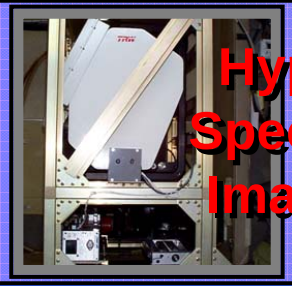
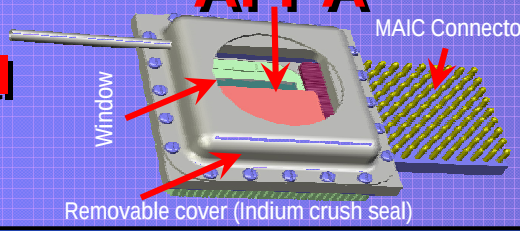
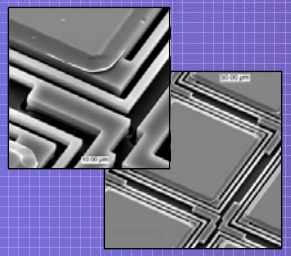
- **Day/Night Imagers**
- **Mega Pixal IR-FPAs**
- **Curved Focal Plane Arrays**

# Opening MEMS Frontiers



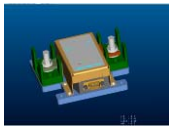

Modified from a slide from
YC Tai, Caltech

# Integrated Microsystems

| Macro | Micro | Key Technology |
|---|---|---|
|  NIST F-1 Cesium Atomic Clock<br>NIST Atomic Clock | CSAC  |  <br>•MEMS Thermal Chamber<br>•VCSEL<br>•Detector<br>•MEMS resonator<br>•Control Electronics |
|  <br>BAWS | SUVOS  2 in. |  UV Lasers  UV LEDs<br>• Ultra Violet Lasers<br>• Ultra Violet Light Emitting Diodes (LEDs) |
|  <br>GC / MS | MGA  |  <br>• MEMS Separation Column<br>• Pre-concentration<br>• MEMS cantilever mass sensor |
|  <br>Hyper Spectral Imager | AFPA  MAIC Connector Window Removable cover (Indium crush seal) |  <br>•Tunable IR filters<br>•Anti-reflection coatings<br>•Thermal matched materials |

# Avionics Today …
# Avionics Tomorrow: Chip-Scale Avionics?

Legacy hardware from F-35 and F-22 programs



**CSA** (HS)

**2 MMCs**
**(Smiths)**

**9 Remote Input Output Units (Smiths)**

**Fuel Probes and Sensors (Smiths)**

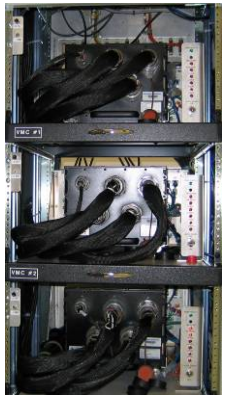
**Voltage Converter** (HS)

**Emergency Gen** (HS)

**Emergency GCU (HS)**

**Non-Linear Inverter** (HS)

**SMU**



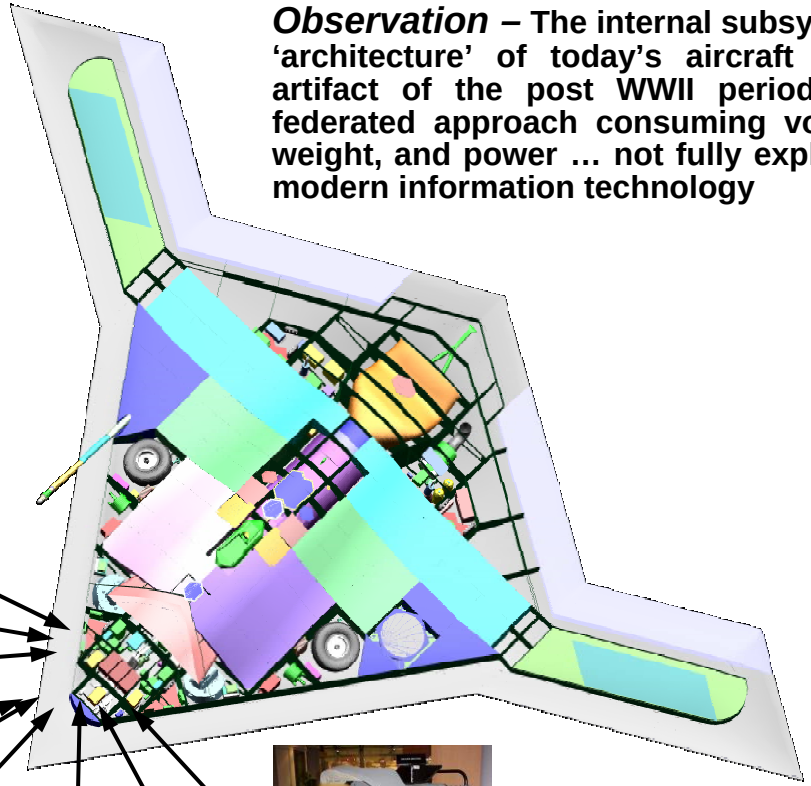
**3 VMCs (Smiths VMC 182900 - 001)**

**3 INS/GPS**
**(Honeywell H-764ACE)**

**TTNT**
**(Rockwell Collins)**

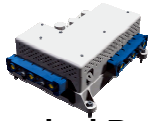
**ARC-210s**
**(Rockwell Collins Model 1851)**

**MIDS**
**(Rockwell Collins LVT 3)**



***Observation* – The internal subsystems 'architecture' of today's aircraft is an artifact of the post WWII period … a federated approach consuming volume, weight, and power … not fully exploiting modern information technology**

**AESA (NGC/Raytheon)**

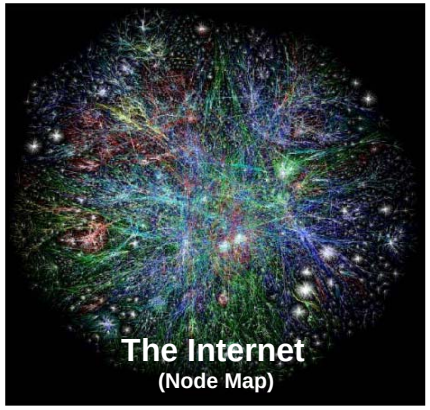


**Electrical Power Distribution Unit**
**(Smiths)**

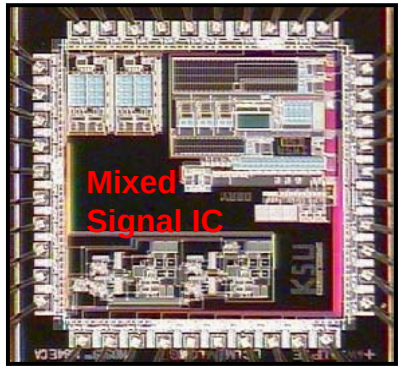
**Network Daughter Board**
**(Smiths)**

# Complex Systems Architectures (more than just the components)


**Complicated:** Many pieces, but the whole can be reassembled from its parts. A key flaw brings the entire system to a halt.






**Complex:** Overall performance can not be represented via reduction to "sum of the part". Complex systems are adaptive, self-organizing, and emergent.

**Challenge: How do we know when a Microsystem is optimum?**

# Path towards Intelligent Microsystems


- **Intelligent: High level of autonomy with the ability to reason and learn with time**

- **Adaptive: Some degree of autonomy to self optimize, test, or monitor. Able to change mode of operation.**

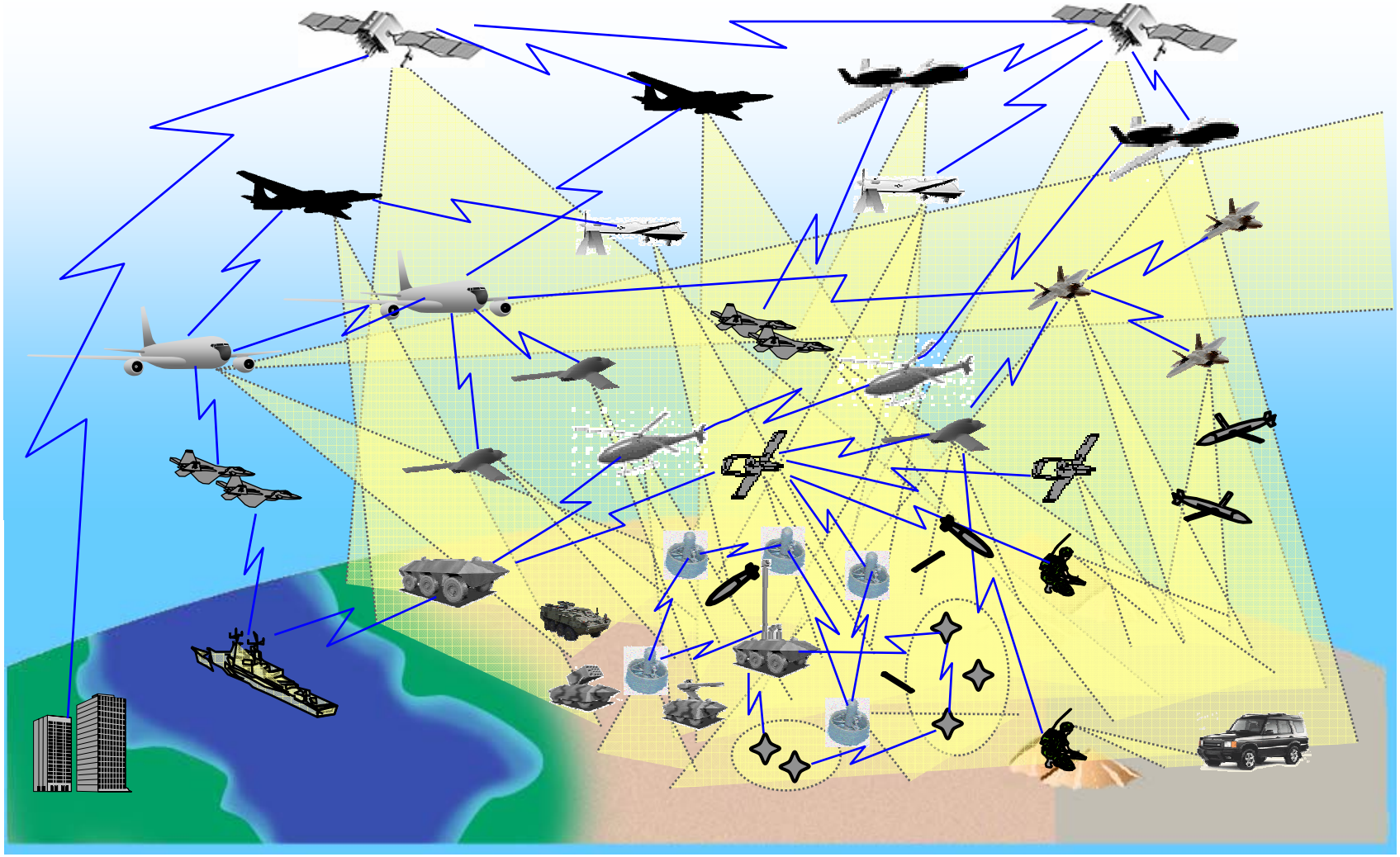
- **Reconfigurable: Predefined, deterministic set of operating parameters that can be selected externally.**

- **Static: Fabricated to design specifications with fixed performance.**

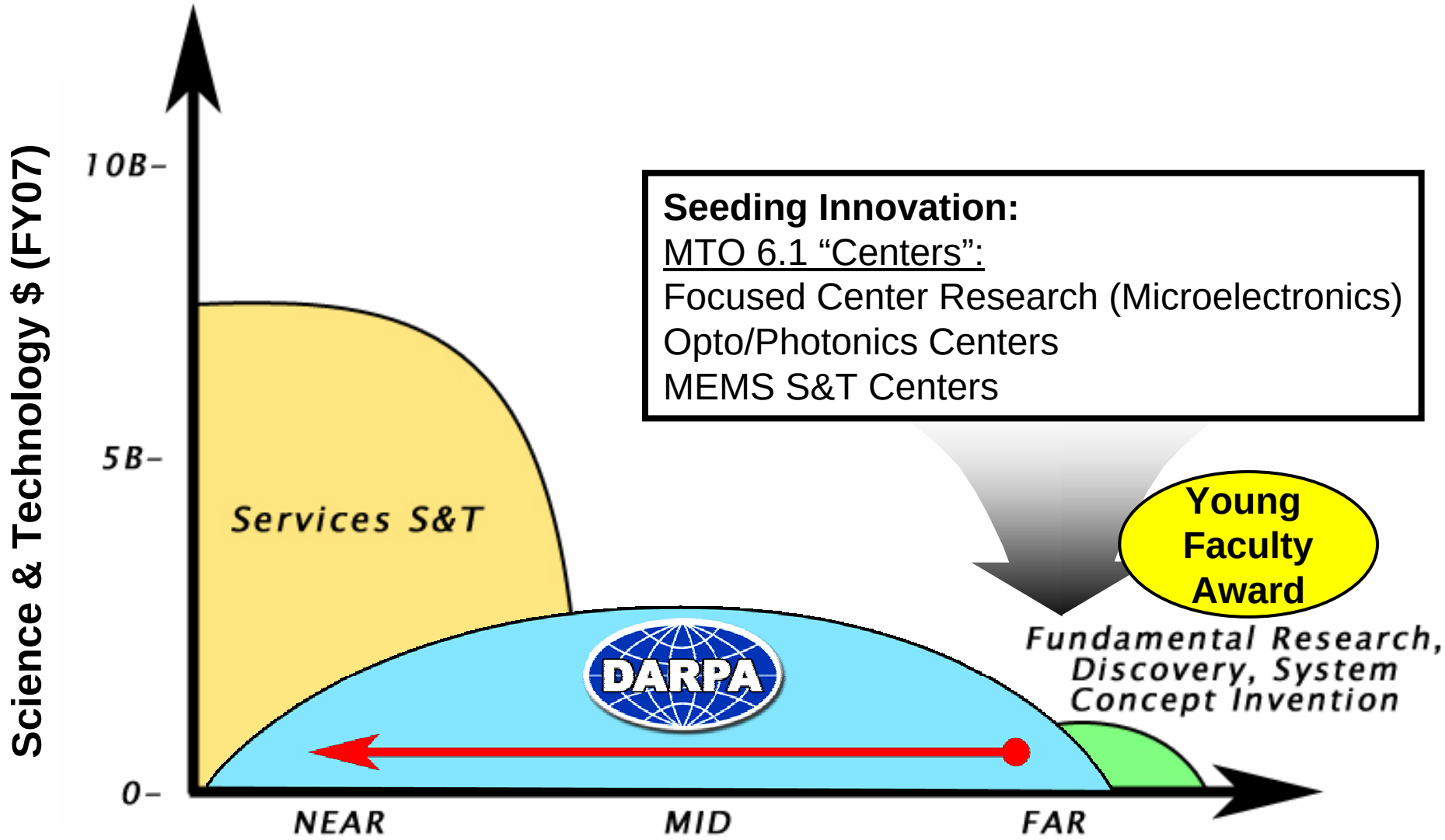
*Current Systems*

# Information Technology: Complex Networks

## Integrated Microsystems are the Networks Foundation



# MTO Basic Research Centers



# Open Challenges

## Sensing

- Single photon detection over SW/MW/LW IR
- Room temperature broadband sensing
- Chip-scale hyper-spectral sensing
- Sub-wavelength-size pixel focal planes
- Ideal Array
- Efficiency

## Processing

- Heat dissipation
- Latency
- Complexity in circuit design
- Theoretical limit analog to digital converters

## Communication

- Spectral efficiency
- Reduced latency
- “internet over RF”
- mm-wave communications
- Coherent optical communications

## Actuation

- Chip scale avionics
- Universal MEMS packaging
- Ultra-stable, lower power timing devices
- Robust, Efficient Actuation
- Micro-scale gas and liquid analyzer

## Energize

- Laser diode bar lifetime and reliability
- Diffraction-limited, coherent high-power diode laser arrays
- Smart power management
- Long endurance micro-power generation
- Efficiency, efficiency, efficiency

# DARPA New Initiative Process

Office Director
(Portfolio Manager,
"angel investor")

Program
Manager/
("VC Sector
Expert")

Industry
Government
Universities

Initial Study

Potential Performers

**Step III**
- Program Reviews
- "Go / No Go" Evaluations

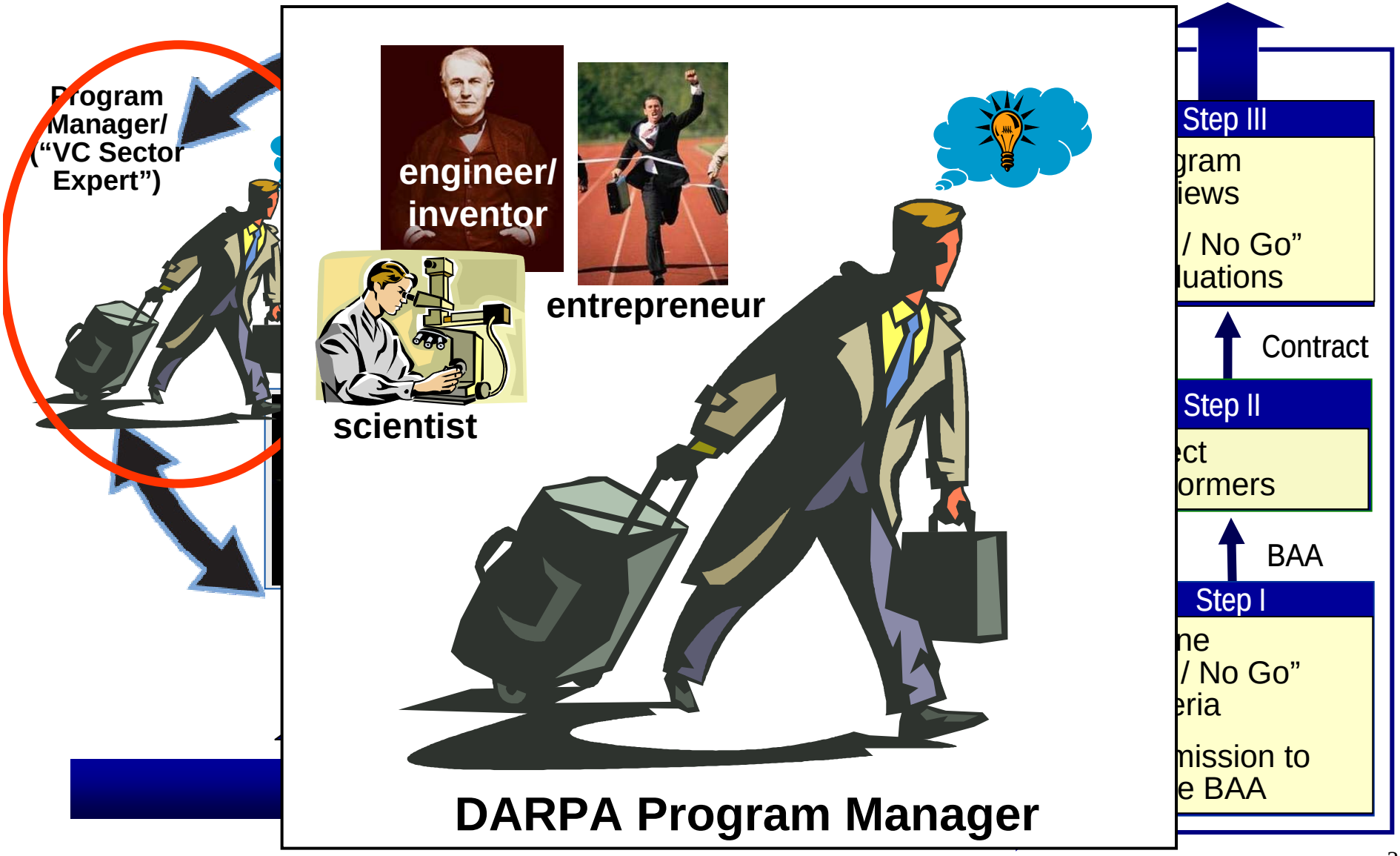
Contract

**Step II**
- Select Performers

BAA

**Step I**
- Define "Go / No Go" Criteria
- Permission to Issue BAA

# DARPA New Initiative Process



# What Has Changed at DARPA?

- **First, what has not changed:**
  - **DARPA's term appointment policy requires a continuous search for new PM's.**
  - **There are many who would like to be DARPA program managers but few who have the skills to succeed.**

- **What has changed:**

- **DARPA's budget has grown by $1 Billion over last 6 years.**

- **DARPA now manages its programs with event driven milestones (Go/NoGo metrics).**

- **The number of programs at DARPA has increased significantly (50% in MTO).**

- **Above requires highly talented technical and entrepreneurial program managers.**

# What Makes a DARPA PM

- **Idea Generator**
- **Technical Expert**
- **Entrepreneur**
- **Passion to Drive Leading Edge Technology**
- **National Service**

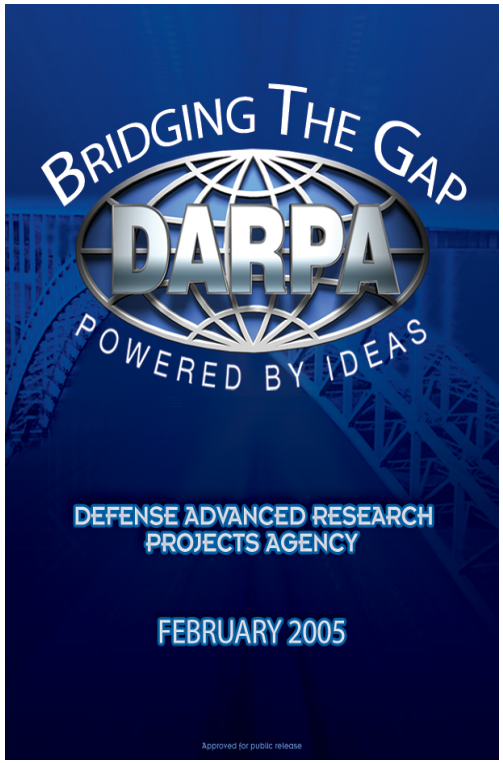
**DARPA Hires Program Managers for their Program Ideas**

**… do you have what it takes?**

**… come talk to me or a PM.**

# The Future

- DARPA Always Interested in Ideas
  - Solicitations: **www.darpa.mil**
  - Talk to DARPA Program Managers
  - Become a DARPA Program Manager
- Upcoming Events
  - 25th DARPA Systems & Technology Symposium (DARPATech 2007) August 7 - 9 2007, Anaheim, California
  - Urban Challenge, November 3, 2007
  - 50th Anniversary Conference / Dinner
    - April 10, 2008. Washington, D.C.




DARPA Overview Pamphlet
www.darpa.mil/body/mission.html


BRIDGING THE GAP
DARPA
1958
2008
50 YEARS
POWERED BY IDEAS